

Amendments to and Listing of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for accelerating a pseudo-random input bit flow having a length of 2^{n-1} bits (PRBS(T_1)), generated from a polynomial of an irreducible degree n at a first relatively-low clock frequency [[f_1]], into an identical output bit flow (PRBS(T_0)) at a second relatively-high clock frequency [[f_0]], greater than the first clock frequency, the method comprising:

collecting the output bit flow;

delaying the collected flow by a predetermined value (τ) respecting the following relation:

$$\tau = ((2^\ell) * T_1) - T_0,$$

wherein T_1 represents the clock period of the input bit flow, T_0 represents the clock period of the output bit flow, and ℓ is an integer setting a decimation parameter, and

combining the delayed flow with the input bit flow in a computer to generate the output bit flow at the second clock frequency.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein delay τ is selected to respect the following relation:

$$\tau = (2k+1) \cdot (2^n - 1) \cdot T_0,$$

where k represents any integer, and where n represents the degree of the irreducible polynomial of the random sequence.

4. (Previously Presented) The method of claim 3, wherein numbers k and ℓ respect the following relation:

$$(2k+1) \cdot (2^n - 1) + 1 = p \cdot 2^\ell,$$

where p is the desired acceleration factor.

5. (Currently Amended) A circuit for accelerating an initial pseudo-random bit flow having a length of 2^{n-1} bits, (PRBS(T_1)) generated from a polynomial of an irreducible degree n at a first relatively-low frequency [[f₁]], into an identical accelerated bit flow (PRBS(T_0)) at a second relatively-high frequency [[f₀]] greater than the first clock frequency, the circuit comprising a combiner having a first input adapted to receive the initial bit flow and having an output adapted to provide the accelerated flow, a second input of the combiner being connected by a delay element to the combiner output, the delay τ of the delay element respecting the following relation:

$$\tau = ((2^\ell) \cdot T_1) - T_0,$$

wherein T_1 represents the clock period of the input bit flow, T_0 represents the clock period of the output bit flow, and ℓ is an integer setting a decimation parameter.

6. (Currently Amended) The circuit of claim 5, further comprising a regeneration circuit configured to shape at the second frequency the output of
~~wherein a reshaping element at the high frequency is provided at the combiner~~
~~output.~~

7. (Previously Presented) The circuit of claim 5, wherein a phase-shifting element is further provided between the generator of the original pseudo-random bit sequence and the combiner.

8. (Previously Presented) The circuit of claim 5, wherein the initial bit flow is obtained by a flip-flop generator.

9. (Currently Amended) The circuit of claim 5, formed by at least one of optical ~~and/or~~ electronic means.

10. (Canceled)